Hardness Assurance Techniques for New Generation COTS Devices*

C. 1. Lee, B. G. Rax, and A. H. Johnston
let Propulsion 1 ,aboratory
California Institute of Technology
Pasadena, CA 91109-8099

Abstract

Hardness Assurance (1 1A) techniques and total dose radiation characterization data for new generation linear and COTS devices from various manufacturer are presented. A bipolar op amp showed significant degradation at HDR, not at low dose rate environment. New generation low-power op amps showed mot-c degradation at low voltage applications. 1 IA test techniques for COTS devices arc presented in this paper.

1. Introduction

New Millennium Program (NM I') is now in progress at JPL. The first of many deep space missions to be flown by the year 2000 under the New Millennium technology validation effort will feature a 1998 launch of a small spacecraft destined for a flyby of an asteroid and a comet. The new lighter and cheaper spacecraft will demonstrate a variety of advanced technologies that help enable many deep space and near Earth missions envisioned by NASA for flight early in the next century. These miniaturized spacecraft will rely heavily on commercial-o - lhc-shelf (COTS) devices rather than high reliability radiation hardened technology devices that were used for former deep space **missions.** In order to usc COTS devices, hardness assurance and radiation testing methods that have been used in the past [1 -S] must be reevaluated to make sure that they arc applicable to the range of commercial technologies that are considered for New Millennium.

Recently many different COTS devices including new generation linear devices from various manufacturers have been radiation tested, Test results indicated that MIL-STD-883 Method 1019.4 works for many conventional CMOS devices. However, it appears to fail for BiCMOS devices and also fails for many bipolar devices. The considerable variation in radiation sensitivity of new generation low-power high-precision linrear devices makes the evaluation of these devices extremely difficult during part selection for space project applications. This paper shows hardness **assurance** test results for various COTS devices. Alternative hardness assurance techniques for COTS devices arc presented in this paper for space applications.

11. 1 lardness Assurance (I 1 A) Test Results

1. A D847 (Low Power Op Amp)

The AD847 is a high-speed, low-power monolithic operational amplifier (Op Amp) which is fabricated with Analog Devices (ADI) junc[icm-isolated complementary-bipolar (CB) process, Laser wafer trimming is used to reduce the input offset voltage. The maximum specification input offset voltage is 1 mV at room temperature, and 3.5 mV over commercial temperature range.

During high dose rate (1 IDR), 25 rad(Si)/s testing, the input offset voltage degraded severely at very low radiation levels as shown in Figure 1. These changes were so large -20 to 30 mV at radiation levels above 10 krad(Si) - that circuit failure would result in many applications, Unbiased devices show very little degradation up to the final total dose level of 30 krad(Si). The large changes in offset voltage recovered after irradiation, when the annealing was clone at room temperature and high temperature. This is much different than the behavior of other bipolar linear circuits which exhibit little or no annealing, and much less difference between biased and unbiased results. In contrast with the biased offset voltage results in Figure 1, unlike most bipolar op-amps, input bias current showed insignificant degradation.

Testing at 0.002 rad(Si)/s was conducted to observe low dose rate (1 ,DR) effects on this linear device. Devices were

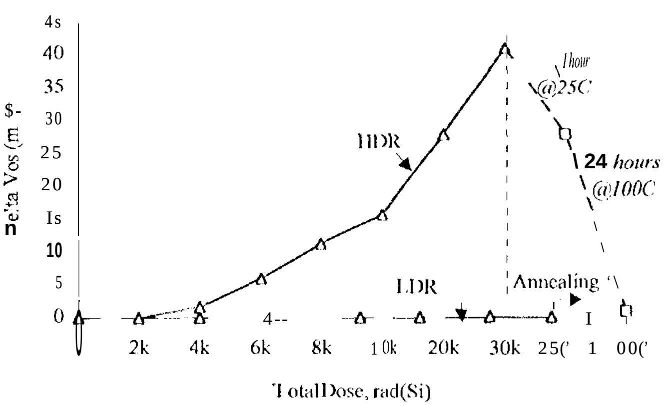

Figure 1. Change in input offset voltage of AD847 at HDR of 25 rad(Si)/s and LDR of 0.002 rad(Si)/s.

* The work described in **this paper** was **carried** out **by** the Jet Propulsion Laboratory, California Institute of Technology, under contract with the National Aeronautics and **Space** Administration Code Q. Work funded by the **NASA** Microelectronics Space Radiation Effects Program (MSREP).

irradiated to 30 krad(Si) and the input offset voltage changed only a few tenths of a millivolt as shown in Figure 1. All other parameters showed insignificant degradation at 30 krad(Si) during the low close rate testing. It could be predicted that due to the fast annealing characteristic, this device should perform better at LDR. However, this is a bipolar linear device not a CMOS device, and the mechanism for the large change in offset voltage during HDR testing is a new effect cm bipolar family of devices. The stucture of the base-emitterjunction is little different than those affected by LDR irradiation. Even though the it has rather thick base-emit[crjunction, the structure looks quite different. The junction is tappered sharply to the SiO_2 emitter.

2. *A 1>101'284 (Low Voltage Op Amp)*

OP284 is a new generation of rail-to-rail op amp that operates with a single power supply. This low voltage and precision op amp is specially attractive to circuit designers of power sensitive systems such as New Millennium Program. This op amp can be operated at 3V and 5V single power supplies and also conventional ±15V applications.

Total dose irradiation at 100 rad(Si)/s was performed and devices were biased with a single power supply, 5V. Offset voltage and input bias currents were most sensitive parameters. Offset voltages at three different supply voltages were measured after cacb irradiation and shown in Figure 3. Significant degradation was observed at lower voltage applications, the offset voltage exceeded the specification limit (200 uA) at below I O krad(Si). However, the offset voltage al 15V application showed that devices were witbin tbc specification limit up to the total dose level of about 90 krad(Si).

input bias current also degraded significantly for all three supply voltages, it exceeded tbc specification limit (500 nA) at below 10 krad(Si) and gradually increased to 2300 nA at 100 krad(Si). These arc new results on these family of bipolar op-amps with high dose rate irradiation. This much severe degradation was not observed with old conventional, high power bipolar op-amps.

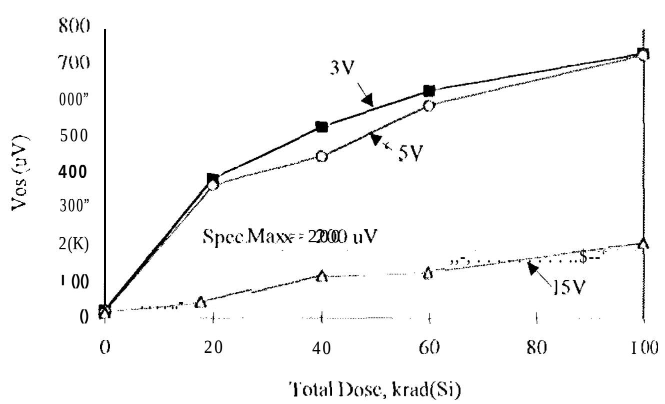

Figure 3. OP284 Offset voltage degradation with HDR of 100 rad(Si)/s at three different power supply voltages.

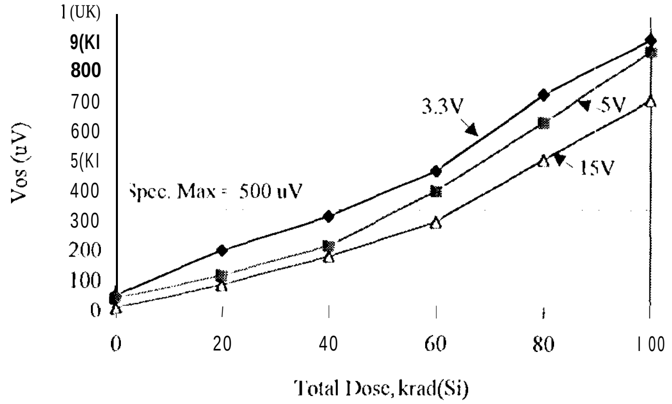

Figure 4. Offset voltage degradation of LT1211 dual op-amp at three different power supply voltages during HDR, 100 rad(Si)/s, irradiation.

Because this device was manufactured for low voltage applications, a test was conducted to find the lowest supply voltage that device would be still functional. The lowest operational supply voltage was 1.9 V and the functional supply voltage remained at 1.9 V with the total dose level up to the 100 krad(Si).

3.1.7'1211 (*Single Supply Dual Precision Op Amp*)

A similar device, 1,'1'1211, low voltage op-amp, manufacutered by Linear Technolgy (LT) was tested and biased with 5V during irradiation. This op amp is specified of I single 3.3V, single 5V and ±15V supply voltages. It operates on a supply voltage greater than 2.5V and requires only 1.3 mA of quiescent supply current per op amp. Offset volatge degraded similar fashion as the previous ADIOP284 and s}1owccI more degradation at lower voltages 3V and 5V as shown in Figure 4.

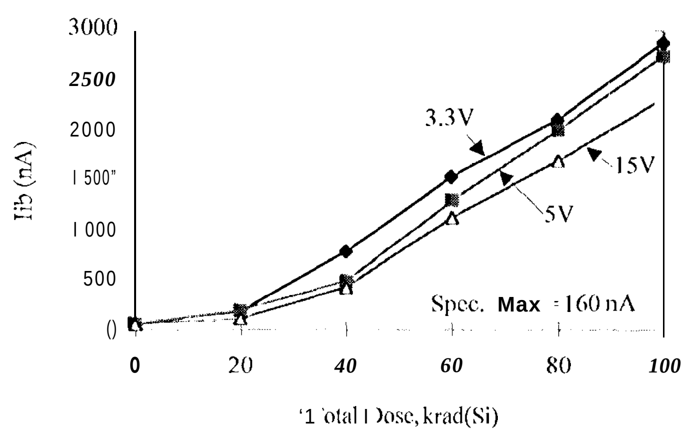

Figure 5. input bias current degradation of 1,'1'1211 dual op-amp at three different supply voltages during 1 HDR, 100 rad(Si)/s, irradiation.

This device has excellent dc precisions and it features low input offset voltage, input offset current, and input bias current. However, this is new generation low-power high-precision op amp showed singnificant degradation with a high close rate irradiation compared to the old conventional op-amps. The input bias current degraded significantly at below 5 krad(Si) as shown in Figure S and reached almost 3000 nA at 100 krad(Si) during HDR testing of 100 rad(Si)/s.

4. LMC6462 (Dual Micropower CMOS Op Amp)

The National Semiconductors LMC6462 is a micropower version of the conventional LMC6482. This device is guaranteed specifications at 3V and 5V low voltage applications. Input current of 150 fA and low input offset voltage of 0.25 mV are achieved with CMOS architecture.

ofl'set voltage exceeded the specification limits below 10 krad(Si) and continually increased up to the total dose level of 15 krad(Si) as shown in Figure 6. At that total dose level, the device was no longer functional. The output high parameter could not be measured because the output was stuck at low.

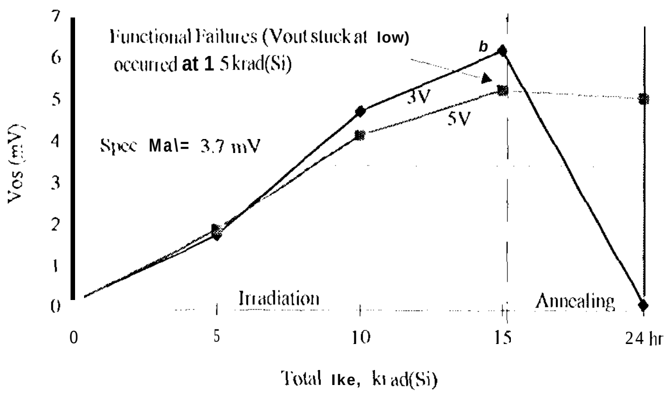

Figure 6. Comparison of input offset voltage of LMC6462 CMOS op-amp at 3V and 5V supplies and annealing.

110WCVCI, due to the low voltage feature, the offset voltage of the op amp was able to measure after the device failure. Even though the offset voltages with 3V measurements recovered after 24 hours annealing at room temperature, the functionality of the output did not recover at all. The offset voltage at 5V did not show much annealing after room temperature annealing and the output was still stack low and the op amp was non-functional.

The input bias current showed similar reponses at both 3V and 5V supplies and annealed with room temperature as shown in Figure 7. The output stuck at low level at 15 krad(Si) and devices were non-functional.

This CMOS op amp also showed more degradation at 3V, lower voltage than 5V supply voltage. This is a consistent results observed with bipolar low voltage op amps that previously discussed. It seems that regardless of technologies, total dose

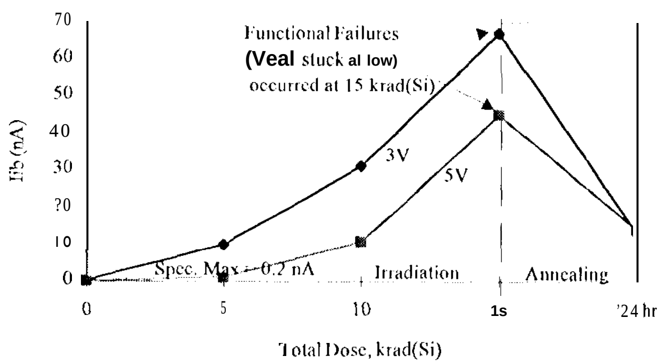

Figure 7. Comparison of input bias current of LMC6462 CMOS op-amp at 3V and 5V supplies and annealing.

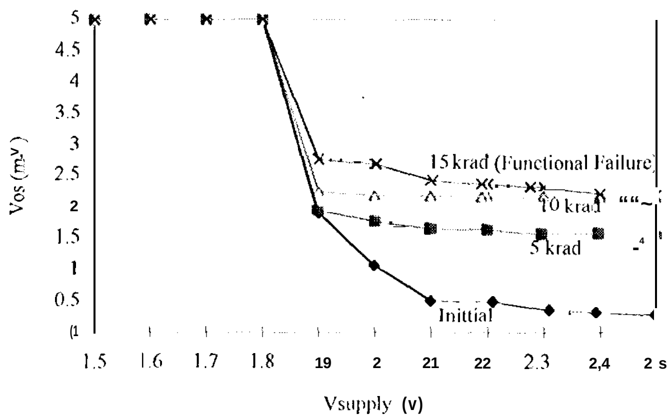

Figure 8. LMC6462 input offset voltage measured at various supply voltages.

degradation is more severe at lower voltages. 'This new response is somewhat disturbing for the new age, low-power small space Systems.

The offset voltage versus supply voltage was measured to verify the lowest voltage the device would be still functional and it is shown in Figure 8. The lowest operational supply voltage was about 2.1 V. However as the total dose radiation level increases the input offset voltage continuously increased until devices became non-functional at 15 krad(Si).

5. 01'42 *(Bipolar Op Amp with JFET input)*

OP42 is a bipolar 0p Amp with a JFET input stage. The input offset voltage degraded significantly more at LDR of 0.005 rad(Si)/s compared to the intermediate dose rate of 0.124 rad(Si)/s. The change in input offset voltage is approximately a factor of four greater at low dose rate and it is shown in Figure 9.

This is consistent with results for dose rate sensitivity of bipolar op amps. Most other parameters were within specification limits at 25 krad(Si). However, this is not sufficient to determine whether the device would be even more sensitive to

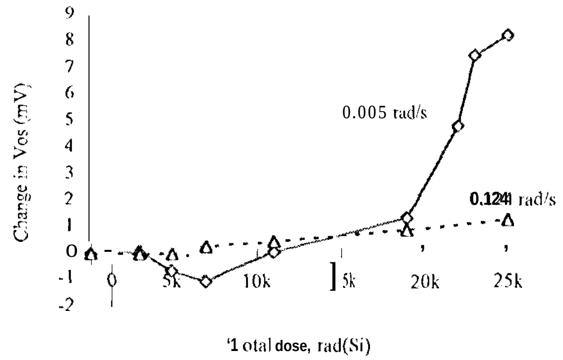

Figure 9. Comparison of input offset voltage at intermediate and low dose rates for OP42.

the input offset voltage changes at much lower dose rates. Very low dose rate (VLDR) testing of 0.001 rad(Si)/s is in progress to further investigate degradation of the offset voltage and the results will be included in the final paper.

6. MX674A (BiCMOS 12-bit ADC)

This Maxim 12-bit A/D converter is fabricated with a BiCMOS process. A number of different tests were performed on this device, using a wide range of dose rates. This is a complex device which contains bipolar and MOS circuit elements. The total dose radiation failure levels and failure modes of the converter are quite different under different dose rate conditions as shown in Figure 10. It appears that MOS-related mechanisms dominate the device response at high dose rates, while bipolar related mechanisms dominate at low dose rates.

At high dose rate, a gradual increase in tri-state leakage current was observed, followed by functional failure at 20-22 krad(Si). [6] Complete recovery occurred when devices were annealed at 100 °C. Tests at 0.1 rad(Si)/s appeared to be consistent with the results at high dose rate. The failure level

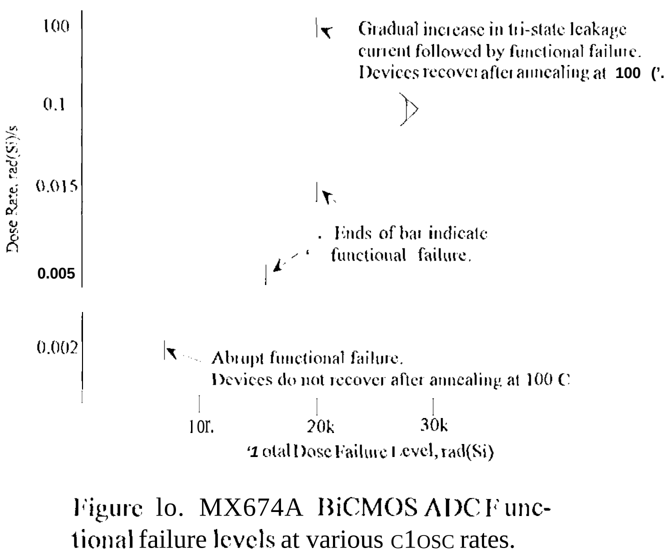

Figure 10. MX674A BiCMOS ADC Functional failure levels at various dose rates.

increased to levels above 27 krad(Si), which would be expected because of annealing characteristics of CMOS components.

New test results at VLDR showed that functional failure occurred abruptly between 6 and 7 krad(Si). No electrical parameters changed prior to failure in the VLDR tests. In addition, the devices did not recover after high temperature annealing, even though they had been irradiated to 1/3 the radiation level of the devices used for high dose-rate tests. The low dose-rate failure mechanism was also very sensitive to dose rate. At 0.005 rad(Si)/s functional failure did not occur until approximately 15 krad(Si). This is not only clear evidence of a different internal failure mechanism, but it also suggests that the lower failure level is caused by dose-rate effects in the bipolar transistors. If the VLDR failure was caused by MOS transistors, then the devices should also fail after high temperature rebound tests.

The distinct differences in the failure level of devices tested at 0.005 rad(Si)/s and 0.002 rad(Si)/s, may indicate that the dose rate was not sufficiently low to eliminate the dose rate sensitivity. Therefore, it is possible that these converters will fail at even lower total dose radiation levels when they are irradiated at dose rates below 0.002 rad(Si)/s. Similar behavior has been observed for bipolar linear devices at dose rates below 0.005 rad(Si)/s. [7]

The failure mode of this device at high dose rates was consistent with CMOS failure mechanisms. Devices recovered completely after high temperature annealing. However, applying Method 1019.4 would clearly overestimate the hardness level of this device. Testing at high and low dose rates provides a secondary check on the adequacy of 1019.4 provided the low dose rate is sufficiently low to reveal the second failure mode, or failure at lower levels than under high dose rate test conditions. Dose rate between 0.1 and 1 rad(Si)/s would not be adequate, but dose rates of 0.02 rad(Si)/s or lower would be effective provided the results were properly interpreted. The key is to compare the failure modes at high and low dose rates, along with the failure levels under the two different conditions. If the failure mode is different at the lower dose rate, it will show that there is a low dose-rate problem, requiring further investigation.

4. McCoy 00136 (CMOS Crystal Oscillator)

McCoy 16 MHz crystal oscillators were tested at 0.002 rad(Si)/s. These are hybrid devices with an internal CMOS integrated circuit. Very slight changes in frequency were observed at low total dose levels. The oscillators failed catastrophically at very low radiation levels as shows in Figure 11, No parametric changes occurred prior to catastrophic failures except the very slight shift in frequency. Devices did not recover during room and high temperature annealing tests. The catastrophic functional failure at low total dose level with VLDR, inconsistent supply current measurements at the failure level, and the different annealing response make it difficult to use this device in space applications, unless the required radiation level is below 5 krad(Si).

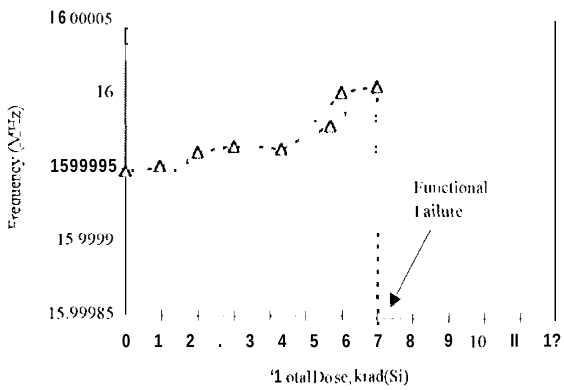

Figure 11. McCoy 00136 crystal oscillator LDR test result

There were unit-to-unit differences in the failure level, ranging from 7 to 10 krad(Si). The McCoy oscillator is an example of a part with extreme sensitivity to ionizing radiation. High dose rate testing along with post-radiation tests will be done for the final paper to see whether Method 1019.4 would be effective for this device or not.

5. CS5016 (CMOS 16-bit ADC)

This CMOS converter behaved as expected and followed the conventional CMOS device radiation degradation mechanism. The low failure level with a high dose rate of 50 rad(Si)/s, about 4-5 krad(Si), recovery with room temperature and high temperature annealing, and an order of magnitude improved failure level with a low dose rate test, 0.005 rad(Si)/s, indicated that the Method 1019.4 would work for this CMOS converter.

The most critical and sensitive parameter, signal-to-noise ratio (SNR) degraded gradually with increasing levels of radiation, as shown in Figure 12. At 40 krad(Si), SNR decreased by approximately 7 dB for biased devices. Unlike other electrical parameters, SNR did not recover after room and high temperature annealing tests. Unbiased devices showed insignificant degradation in SNR. Devices had initial values of SNR that were

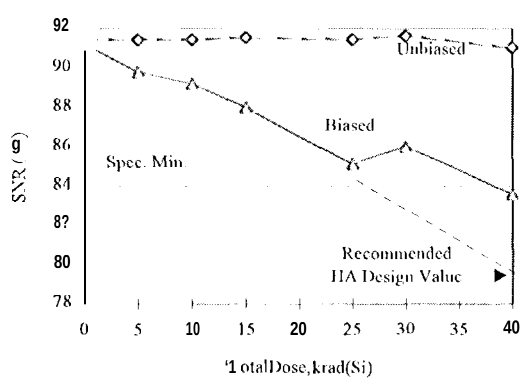

Figure 12. [SS016 16-bit ADC SNR degradation with dose rate of 0.005 rad(Si)/s.

well above the minimum specification value. In order to account for variations in initial SNR between devices, some space applications had to use 80 dB as a post radiation HA design value.

III. Discussion

Total close radiation degradation depends on a number of factors, including bias conditions, operating voltages, oxide thickness, physical device structure, and processing. Some technologies are also affected by dose rate. Low dose rate effects are a critical factor in many linear bipolar integrated circuits, [7-10] adding further difficulty to the already complex problem of interpreting radiation test results. These difficulties can be particularly severe in mixed technology devices such as BiCMOS.

Many bipolar op-amps degrade more severely at low dose rates with little or no annealing. However, the AD847 behaves quite differently, degrading severely at high dose rate and annealing rapidly, even at room temperature. Input bias current did not change significantly, but very large changes occurred in input offset voltage. This failure mechanism was not expected for this device. Low dose rate test results indicates that devices are not affected by low dose rate irradiation. Different physical structure of the device compared to the more conventional bipolar devices is the major factor for the different results.

OP284 and 1,'1'1'211 are new generation high-precision op amps can be used in low-voltage, extremely low-power applications. However, total dose radiation degradation is much more severe at low voltage application, This raises another issue for future smaller, lighter, and low-powered space systems,

A CMOS micropower op amp, LMC6462 is another ideal candidate device which would be used in NM I'. Not only parametric failures were observed at low total dose radiation level, the functional failure was observed at low level as well. The functional failure remained during anealing. This indicates that the low dose rate environment would not improve the failure level of this device.

Total dose test results of a BiCMOS A/D converter, MX674A clearly show that the device has different failure modes at high, intermediate, and low dose rates. The failure mechanism appears to be very sensitive to dose rate effects, probably because of the bipolar components that are used in internal circuitry of the device. Total dose degradation at low dose rate was the same for biased and unbiased devices, but this was not the case for irradiation at high dose rate. This suggests that bias condition may be an additional useful tool for hardness assurance.

IV. Hardness Assurance Techniques

Reliability and design assurance are critical tasks for successful space missions. COTS devices present a number of difficulties because less information is available about their fabrication, and no explicit controls are present for radiation tolerance. Hardness assurance testing of these commercial

'1 'able 1. 11A Techniques for COTS Devices

Dev ice	Function	Tech.	Failure Level krad(Si)	Method 1019,4 works?	11A Techniques
Ad847	Op Amp	Bipolar	4	No	Mixed DR
OP284	Op Amp	Bipolar	10	Yes	
1"1'1?11	Op Amp	Bipolar	5	Yes	
LMC6462	Op Amp	CMOS	2	Nrr	
OP42	Op Amp	Bipolar/ JFET input	20	No	Mixed DR
MX674A	ADC	BiCMOS	6	No	"
MC136	oscillator	CMOS	7	No	"
CS5016	ADC	CMOS	4	OK	......

devices is more important than ever because of the extreme sensitivity of these devices in radiation environments. In many cases, tests must be done with small sample sizes and limited understanding of device technology information. '1'able 1 summarizes the COTS devices with various different technologies tested for this paper. Most of them failed at fairly low total dose levels and cannot be adequately tested with Method 1019.4.

At this point there is no reason to doubt the applicability of Method 1019.4 for CMOS devices. However, as noted by others, it is not always a reliable approach for bipolar devices. The results for the MX674A also show that Method 1019.4 may also fail for BiCMOS devices. The dominance of CMOS failure modes at high dose rate for the MX674A can mask bipolar failure modes that only appear at low dose rate, providing a misleading picture of the applicability of the test method. For COTS devices these is the added complication] that it may not always be possible to get reliable in formation about device technologies. Hybrid devices arc particularly troublesome because they may contain a mix of bipolar and CMOS technologies.

One alternative approach which is being used at J]'], for COTS devices uses tests at two different dose rates. The lower dose rate does not have to be low enough to eliminate dose-rate sensitivity, only to show that the result is inconsistent with initial dose rate tests. The key to its success is careful evaluation of the results at the lower dose rate. Specific steps in this procedure arc outlined below:

1. High ciosc-rate testing, followed by annealing as specified in Method 1019.4

2. Tests at a low dose rate, 0.005 to ().015 rad(Si)/s

3. (comparisons of failure levels and failure modes of results at the two dose rates

This approach appears to be feasible for devices with modest total dose requirements (below 20 krad(Si)), where the low dose-rate tests can be completed in reasonable time periods, but would not be appropriate for devices that must withstand very high radiation levels. The approach appears to work for several different bipolar and BiCMOS devices. Data will be included in the full paper on fifteen different device types where this approach has been used. Specific parts include the five parts in '1'able 1, two sample-aad-hold circuits, an additional A/D converter, and several bipolar devices.

V, References

[1]. F. W. Sexton, et al., "Qualifying, Commercial ICs for Space Total Dose Environments", IEEE Trans. Nucl. Sci., NS-39, 1869(1992).

[2], D. M. Fleetwood, P. S. Winoker, aad '1. 1. Meisenheimer, "Hardness Assurance for Low-Dose Space Applications", IEEE Trans. Nucl. Sci., NS-38, 1552 (1991).

[3]. D. M. Fleetwood, et al., "An Improved Standard Total Dose Test for CMOS Space Electronics", IEEE Trans. Nucl. Sci., NS-36, 1963 (1989),

[4]. P. S. Winoker, M. R. Shaneyfelt, 'T. L. Meisenheimers, and D. M. Fleetwood, "Advanced Qualification Technologies," Proceedings of the 1993 RADECS Conferacc, IEEE Doc. 93'1'110616-3, 289(1993).

[5]. L. Henderson, et al., "A Practical System Hardware Assurance Program", IEEE Trans. Nucl. Sci., NS-40, 1725 (1993).

[6]. C. 1. Lee, B. G. Rax, and A. H. Johnston, "Total Ionizing Dose Effects ia 12-bit Successive-Approximation Analog-to-Digital Converters," IEEE Work shop Record, Radiation Effects Data Workshop, I 12 (1 993).

[7]. A. H. Johnston, B. G. Rax, and C. 1.1 .ee, "Total Dose Effects in Conventional Bipolar Transistors and Linear Integrated Circuits", IEEE Trans. Nucl. Sci., NS-42, 1650 (1995).

[8]. D. M. Fleetwood, et al., "Enhanced Charge Trapping in Bipolar Spacer Oxides During Low Dose-Rate Irradiation," IEEE Trans. Nucl. Sci., NS-41, 1871 (1994).

[9]. S. McClure, R. 1. l'case, W. Will, and G. Perry, "Dependence of Total Dose Response of Bipolar Linear Microcircuits on Applied Dose Rate", IEEE Trans. Nucl. Sci., NS-41, 2544 (1994).

[10]. T. Carrirer, J. Beaucour, A. Gach, B. Johlander, and L. Adams, "Dose Rate and Annealing Effects on Total Dose Response of MOS and Bipolar Circuits", IEEE Trans. Nucl. Sci., NS-42, 1567 (199 S).